Constant-round interactive proof systems for AC0[2] and NC1

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Abstract. We present constant-round interactive proof systems for sufficiently uniform versions of $\mathcal{AC}^0[2]$ and $\mathcal{NC}^1$. Both proof systems are doubly-efficient, and offer a better trade-off between the round complexity and the total communication than the work of Reingold, Rothblum, and Rothblum (*STOC*, 2016). Our proof system for $\mathcal{AC}^0[2]$ supports a more relaxed notion of uniformity and offers a better trade-off between the number of rounds and the round complexity that our proof system for $\mathcal{NC}^1$. We observe that all three aforementioned systems yield constant-round doubly-efficient proof systems for the All-Pairs Shortest Paths problem.

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1 Introduction

The notion of interactive proof systems, put forward by Goldwasser, Micali, and Rackoff [9], and the demonstration of their power by Lund, Fortnow, Karloff, and Nisan [12] and Shamir [16] are among the most celebrated achievements of complexity theory. Recall that an interactive proof system for a set S is associated with an interactive verification procedure, V, that can be made to accept any input in S but no input outside of S. That is, there exists an interactive strategy for the prover that makes V accepts any input in S, but no strategy can make V accept an input outside of S, except with negligible probability. (See [3, Chap. 9] for a formal definition as well as a wider perspective.)

The original definition does not restrict the complexity of the strategy of the prescribed prover and the constructions of [12, 16] use prover strategies of high complexity. Seeking to make interactive proof systems available for a wider range of applications, Goldwasser, Kalai and Rothblum [8] put forward a notion of *doubly-efficient* interactive proof systems. In these proof systems the prescribed prover strategy can be implemented in polynomial-time and the verifier's strategy can be implemented in almost-linear-time. (We stress that unlike in *argument systems*, the soundness condition holds for all possible cheating strategies, and not only for feasible ones.) Restricting the prescribed prover to run in polynomial-time implies that such systems may exist only for sets in $\mathcal{BPP}$, and thus a polynomial-time verifier can check membership in such sets by itself. However, restricting the verifier to run in almost-linear-time implies

that something can be gained by interacting with a more powerful prover, even though the latter is restricted to polynomial-time.

The potential applicability of doubly-efficient interactive proof systems was demonstrated by Goldwasser, Kalai and Rothblum [8], who constructed such proof systems for any set that has log-space uniform circuits of bounded depth (e.g., log-space uniform $\mathcal{NC}$). A more recent work of Reingold, Rothblum, and Rothblum [15] provided such (constant-round) proof systems for any set that can be decided in polynomial-time and a bounded amount of space (e.g., for all sets in $\mathcal{SC}$). In our prior works [5, 7], we presented simpler and more efficient constructions of doubly-efficient interactive proof systems for some special cases: In particular, in [5] we considered a class of "locally-characterizable sets", and in [7] we considered the problem of counting t-cliques in graphs.

In this work we consider the construction of constant-round doubly-efficient interactive proof systems for (sufficiently uniform) versions of $\mathcal{AC}^0[2]$ and $\mathcal{NC}^1$. We mention that the proof systems for $\mathcal{NC}$ constucted by Goldwasser, Kalai and Rothblum [8] use $O(d(n)\log n)$ rounds, where $d(n)$ is the depth of the n^{th} circuit. Building on their techniques, Kalai and Rothblum have observed the existence of a constant-round proof system for a highly-uniform version of $\mathcal{NC}^1$, but their notion of uniformity was quite imposing and they never published their work [11]. In Section 3, we use similar ideas towards presenting a constant-round proof system for a sufficiently uniform version of $\mathcal{NC}^1$, which we believe to be less imposing (see also the overview in Section 1.4), but our main contribution is in presenting such a proof system for a sufficiently uniform version of $\mathcal{AC}^0[2]$: The latter proof system is more efficient and refers to a more relaxed notion of uniformity.

1.1 Our main result: A proof system for $\mathcal{AC}^0[2]$

We present constant-round doubly-efficient interactive proof systems for sets acceptable by (sufficiently uniform) constant-depth polynomial-size Boolean circuits of unbounded fan-in and parity gates (i.e., the class $\mathcal{AC}^0[2]$). Note that this class contains "seemingly hard problems in $\mathcal{P}$" (e.g., the t-CLIQUE problem for n-vertex graphs can be expressed as a highly uniform DNF with n^t terms (each depending on $\binom{t}{2}$ variables)). Postponing, for a moment, a clarification of what is meant by "sufficiently uniform", our result reads

Theorem 1.1 (constant-round doubly-efficient interactive proofs for $\mathcal{AC}^0[2]$, loosely stated): *For constants $c, d \in \mathbb{N}$, suppose that $\{C_n : \{0,1\}^n \to \{0,1\}\}$ is a sufficiently uniform family of Boolean circuits with unbounded fan-in parity and conjunction gates such that C_n has size at most n^c and depth d. Then, for every $\delta \in (0,1]$, the set $\{x : C_{|x|}(x)=1\}$ has a $O(cd/\delta)$-round interactive proof system in which the verifier runs in time $O(n^{1+o(1)})$, the prescribed prover can be implemented in time $O(n^{c+o(1)})$, and the total communication is n^δ.*

We mention that the work of Reingold, Rothblum, and Rothblum [15] implies that log-space uniform $\mathcal{AC}^0[2]$ (actually, even log-space uniform $\mathcal{NC}^1$)[1] has constant-round doubly-efficient interactive proof systems. One advantage of our construction over [15] is that, being tailored to $\mathcal{AC}^0[2]$, it is much simpler and more transparent. In addition, the round complexity of our proof systems is considerably better than the round-complexity in [15]; specifically, we present a $O(1/\delta)$-round system with total communication n^δ, whereas in [15] obtaining total communication n^δ requires $\exp(\widetilde{O}(1/\delta))$ many rounds.

Corollaries. Using Theorem 1.1, we obtain a constant-round doubly-efficient interactive proof system for the *All Pairs Shortest Path* (`APSP`) problem (see background in [18]). Such a proof system follows also from the work of [15], but this fact was not observed before. The key observation is that verifying the value of `APSP` can be reduced to matrix multiplication in the $(\min, +)$-algebra *via a doubly-efficient* NP-proof system.

Recall that matrix multiplication in the $(\min, +)$-algebra refers to the case that multiplication is replace by addition and the sum is replace by the minimum; that is, the product of the matrices $A = (a_{i,j})_{i,j\in[n]}$ and $B = (b_{i,j})_{i,j\in[n]}$, denoted $A * B$, equals $C = (c_{i,j})_{i,j\in[n]}$ such that $c_{i,j} = \min_{k\in[n]}\{a_{i,k} + b_{k,j}\}$ for every $i, j \in [n]$. Given a possibly weighted n-vertex digraph G, we consider the matrix $W = (w_{i,j})_{i,j\in[n]}$ such that $w_{i,j}$ denotes the weight (or length) of the edge from i to j, whereas $w_{i,i} = 0$ and $w_{i,j} = \infty$ if there is no edge from i to j. Then, the shortest paths in G can be read from A^n, and the foregoing NP-proof consists of the prover sending the matrices $A_1, A_2, ..., A_{\lceil \log_2 n\rceil}$ such that $A_0 = A$ and $A_i = A_{i-1} * A_{i-1}$ for all i. Hence, the verification of `APSP` is reduced to the verification of $\log n$ claims regarding matrix multiplication in the $(\min, +)$-algebra, which can be verified in parallel. Focusing on the latter problem, or rather on the set $\{(A, B, A * B) : A, B \in \bigcup_{n\in\mathbb{N}} \mathbb{R}^{n\times n}\}$, we observe that membership can be recognized in $\mathcal{SC}$ (hence the result of [15] applies) as well as by highly uniform $\mathcal{AC}^0$ circuits.

Corollary 1.2 (a constant-round doubly-efficient interactive proof for `APSP`): *Let* `APSP` *consists of pairs* (G, L) *such that* L *is a matrix recoding the lengths of the shortest paths between each pair of vertices in the weighted graph* G*. For every constant* $\delta > 0$*, the* `APSP` *has a* $O(1/\delta)$*-round interactive proof system in which the verifier runs in time* $O(n^{2+o(1)})$*, the prescribed prover can be implemented in time* $O(n^{4+o(1)})$*, where* n *denotes the number of vertices in the graph and weights are restricted to* $[-\exp(n^{o(1)}), \exp(n^{o(1)})]$*. Furthermore, except for the first prover message, in each subsequent round, the prover sends* n^δ *bits.*

As with Theorem 1.1, the application of [15] to `APSP` would have yielded $\exp(\widetilde{O}(1/\delta))$ rounds.

Another problem to which Theorem 1.1 is applicable is the set of graphs having no t-cliques, denoted t-no-`CLIQUE`. For any contant t, constant-round

[1] Actually, the result of [15] can be applied to $\mathcal{NC}^1$ circuits that can be constructed in polynomial time and $n^{o(1)}$-space.

doubly-efficient interactive proof systems for t-no-CLIQUE are implicit or explicit in several prior works. In particular, such proof systems are implied by the aforementioned result of [15] as well as by [5, Sec. 4.3], and were explicitly presented in [7, Sec. 2]. Noting that the said set can be recognized by highly uniform CNFs of size $O(n^t)$ and using Theorem 1.1, we obtain yet another alternative proof system for t-no-CLIQUE.

Corollary 1.3 (a constant-round doubly-efficient interactive proof for t-no-CLIQUE): *For every constants $t \in \mathbb{N}$ and $\delta > 0$, the set t-no-CLIQUE has a $O(t/\delta)$-round interactive proof system in which the verifier runs in time $O(n^{2+o(1)})$, the prescribed prover can be implemented in time $O(n^{t+o(1)})$, and the total communication is n^δ, where n denotes the number of vertices in the graph.*

In the following table, we compare Corollary 1.3 to the prior proof systems known for the t-no-CLIQUE problem.

obtained	(in)	# rounds	total comm.	verifier time	prover time
via $\mathcal{SC}$	[15]	$\exp(\widetilde{O}(1/\delta))$	n^δ	$\widetilde{O}(m)$	$\mathrm{poly}(n^t)$
via "local characterization"	[5]	t/δ	n^δ	$\widetilde{O}(m)$	n^{t+1}
directly	[7]	t	$\widetilde{O}(n)$	$\widetilde{O}(m)$	$n^{0.791t}$
via $\mathcal{AC}^0[2]$	(this work)	$O(t/\delta)$	$n^{\delta+o(1)}$	$n^{2+o(1)}$	$n^{t+o(1)}$

Table 1. Comparison of different constant-round interactive proof systems for the t-no-CLIQUE problem, for the constants t and $\delta > 0$, where n (resp., $m > n$) denotes the number of vertices (resp., edges).

Our proof system for t-no-CLIQUE is very similar to the one in [5]. The difference is that we apply the sum-check protocol to an arithmetic circuit defined over an extension field (of size $n^{2\delta}$) of GF(2), whereas in [5] it is implicitely applied to an arithmetic circuit defined over a field of prime characteristic that is larger than $\binom{n}{t}$. Furthermore, here the arithmetic circuit is a pseudorandom linear combination of the $\binom{n}{t}$ tiny circuits that identify specific t-cliques, whereas in [5] the arithmetic circuit counts these t-cliques.

1.2 Notions of sufficiently uniform circuits

Some notion of uniformity is essential for a result such as Theorem 1.1, since the claim regarding the input x refers to satisfying a $\mathrm{poly}(|x|)$-sized circuit $C_{|x|}$, whereas the verifier is restricted to almost-linear time. In the context of this work, we seek the most liberal notion that we can support.

Our notion of uniformity is stronger than the notion of log-space uniformity used in [8] (let alone even weaker notions of uniformity that can be supported when applying the result of Reingold, Rothblum, and Rothblum [15] (see Footnote 1)). Specifically, we consider the complexity of a succinct (implicit) representation of the circuit, rather than the complexity of constructing the circuit

itself (i.e., its explicit representation). We consider three such succinct representations, where in all cases we denote by n the length of the input to the poly(n)-size circuit, and assume that the circuit is *layered* (in the sense detailed below):

Adjacency predicate: Such a predicate indicates, for each pair of gates (u, v), whether or not gate u is fed by gate v. Specifically, dealing with circuits of size $s(n) = \mathrm{poly}(n)$, we consider the adjacency predicate $\mathtt{adj} : [s(n)] \times [s(n)] \to \{0, 1\}$,

Incidence function: Such a function indicates, for each gate u and index i, the identity of the i^{th} gate that feeds the gate u, where 0 indicates that u is fed by less than i gates. Specifically, for a predetermined fan-in bound $b(n) \leq s(n) - 1$, we consider the incidence function $\mathtt{inc} : [s(n)] \times [b(n)] \to [s(n)] \cup \{0\}$.

Input assignment in canonical formulae: Here we consider a fixed structure of the circuit as a formula, and specify only the input bit assigned to each leaf of the formula, where the same bit is typically assigned to many leaves. The assignment is merely a function from leaf names to bit locations in the input. Specifically, we consider the input assignment function $\mathtt{ia} : [s(n)] \to [n + 2]$, where location $i \in \{n + 1, n + 2\}$ is assigned the constant $i \bmod 2$ in the "augmented" n-bit input (which holds $n + 2$ bits).[2]

In all cases, we assume that the (depth d) circuit is layered in the sense that, for each $i \in [d]$, gates at layer $i - 1$ are fed by gates at layer i only, where layer i consists of all gates at distance i from the output gate. Indeed, the output gate is the only gate at layer 0, and the gates at layer d are called leaves, since they are not fed by gates but are rather assigned input bits.[3] (Indeed, for simplicity, we do not allow leaves at other layers.)[4] Furthermore, when using the adjacency predicate and the incidence function representations, we shall assume that (for each $i \in [n]$) the i^{th} leaf is assigned the i^{th} input bit (and for $i \in \{n + 1, n + 2\}$ the constant $i \bmod 2$ is assigned to the i^{th} leaf); but in the canonical formulae representation the assignment of input bits to leaves is the only aspects of the circuit that varies.

In all three cases, we make two additional simplifying assumptions. The first is that the circuit contains no "negation" gates (i.e., `not`-gates). This can be assumed, without loss of generality, because we can replace `not`-gates by `parity`-gates (fed by the desired gate and the constant 1, which is the reason for allowing

[2] The need to feed both constants arises from the following conventions by which the circuit is layered and all gates in the same layer compute the same functionality.

[3] We stress that the term 'leaf' is used here also in the case that the circuit is not a formula (i.e., does not have a tree structure). One may prefer using the terms 'terminal' or 'source' instead.

[4] This can be assumed, without loss of generality, by replacing such a potential leaf at layer i with an auxiliary path of dummy gates that goes from layer d to layer i so that this path indirectly feeds the value of the desired input bit to the corresponding gate at layer i.

to feed leaves with the constant 1). The second assumption is that, *for each* $i \in [d]$*, all gates at layer* $i-1$ *have the same functionality* (gate-type).[5]

Theorem 1.1 holds under each of the three representations, when requiring that the corresponding function, which implicitly describes the poly(n)-size circuit C_n, can be represented by a formula of size $n^{o(1)}$ than can be constructed in time $n^{1+o(1)}$. (Recall that the input to the latter formula is of length $O(\log n)$.)

1.3 Overview of our main construction

The construction underlying Theorem 1.1 combines a central ingredient of the interactive proof system of Goldwasser, Kalai, and Rothblum [8] with the approximation method of Razborov [14] and Smolensky [17]. Specifically, we first reduce the verification of the claim that the input satisfies the predetermined Boolean circuit to an analogous claim regarding an Arithmetic circuit (over GF(2)) that is derived from the Boolean circuit using the approximation method. The crucial fact is that that *all multiplication gates in the Arithmetic circuit have small fan-in* (whereas the fan-in of addition gates may be large). With high probability, this approximation does not affect the computation on the given input, but it does introduces a "completeness error" in the verification procedure, which we eliminate later (so to obtained perfect completeness).

Next, following [8], we consider a computation of the Arithmetic circuit (on the given input), and encode the values of the gates at each layer by a low degree polynomial over a large (extension) field (of GF(2)). Here we use the fact that, by virtue of the approximation method, the gates in the Arithmetic circuit compute polynomials of low degree, whereas in [8] obtaining low degree polynomials relied on "refreshing the variables" after each layer of the circuit (see also Eq. (15) in Section 3). That is, unlike in [8], we do not use a generic low-degree extension of the Boolean values (computed by the gates of the Boolean circuit), but rather use the polynomials that are computed by the gates of the Arithmetic circuit (i.e., the formal polynomials that are defined by the circuit). More importantly (and in fact crucially), relying on the foregoing uniformity condition, *we express the relation between the values of the gates at adjacent layers* (of the circuit) *by low degree polynomials*. These polynomials are derived from the small Boolean formulas that compute the adjacency relation.

Lastly, following [8], we reduce the verification of a claim regarding the values at layer $i-1$ in the circuit to a claim regarding the values at layer i, by using the Sum-Check protocol in each reduction step. Specifically, we use the Sum-Check protocol with respect to variables in a relatively large alphabet (of size n^{δ}), so that the number of rounds is a constant (i.e., $O(1/\delta)$). Actually, this refers to the way in which addition gates of unbounded fan-in are handled, where each such poly(n)-way addition is written as a sum over a $O(1/\delta)$-long sequence of indices over an alphabet of size n^{δ} (i.e., $\sum_{i\in[m]} T(i)$ is written

[5] This can be assumed, without loss of generality, by replacing each layer by three consecutive layers so that one layer is devoted to `and`-gates, one to `or`-gates, and one to `parity`-gates.

$\sum_{i_1,..,i_t \in [m^{1/t}]} T(i_1,..,i_t)$). In contrast, multiplication gates, which are of logarithmically bounded fan-in, are treated in a straightforward manner (i.e., we branch to verify each of the logarithmically many claimed values).[6]

To summarize: Using the approximation method allows us to replace `or`-gates (and/or `and`-gates) of unbounded fan-in by multiplication gates of logarithmic fan-in, while introducing parity gates of unbounded fan-in. Each layer of parity gates can be handled by the Sum-Check protocol such that each iteration of this protocol cuts the fan-in of the parity gates by a factor of n^δ. The degree bound on which the Sum-Check protocol relies is due to the uniformity of the original Boolean circuit and to the fact that the multiplication gates have small fan-in. Specifically, a sufficient level of uniformity of the Boolean circuit implies an upper bound on the degree of the polynomials that relate the values of the gates at adjacent layers (of the circuit), whereas the small fan-in of the multiplication gates implies an upper bound on the degree of the polynomial that expresses the values of the various gates.

We mention that the idea of using the approximation method towards emulating $\mathcal{AC}^0[2]$ by low degree arithmetic circuits, *in the context of interactive proof systems*, was used before by Kalai and Raz [10]. Both in [10] and here, this causes a (small) error probability (in the completeness condition).[7]

We *regain perfect completeness* by letting the prover point out a gate in which an approximation error occurs (with respect to the input), and prove its claim. That is, we let the verifier accept in case it is convinced of such a claim (of approximation error), which means that we increase the soundness error (rather than introduce a completeness error).

1.4 The proof system for $\mathcal{NC}^1$

Generalizing and somewhat simplifying the proof systems constructed by Goldwasser, Kalai, and Rothblum [8], we obtain constant-round doubly-efficient interactive proof systems for sufficiently uniform $\mathcal{NC}^1$ (specifically, canonical formulas with a sufficiently uniform input assignment function as discussed in Section 1.2). The simplification is due to relying on a stronger notion of uniformity than the one used in [8], whereas the generalization allows us to reduce the round complexity of [8] by a log-squared factor. Recall that, when handling a (bounded fan-in) circuit $C_n : \{0,1\}^n \to \{0,1\}$ of depth $d(n)$, the proof system of [8] has $O(d(n) \cdot \log n)$ rounds. This is due to invoking the Sum-Check Protocol for each layer in the circuit, and using a version that handles summations over the binary

[6] Indeed, we could reduce the verification of these logarithmically many claims to the verification of a single claim, by using a curve that passes through all the points in these claims, as done in [8]. But since here the number of rounds is a constant, we can afford an overhead that is exponential in the number of rounds (i.e., the overhead is $O(\log n)^{d'}$, where d' is the number of layers having multiplication gates).

[7] In contrast, when using the approximation method in the context of worst-case to average-case reduction for the class $\mathcal{AC}^0[2]$ presented in [6, Apdx A.2], the approximation error is absorbed by the (larger) error rate of the average-case solver.

alphabet. Instead, for any constant $\delta > 0$, we invoke the Sum-Check protocol for each block of $\delta \log_2 n$ consecutive layers in the circuit, and use a version that handles summations over an alphabet of size n^δ. Hence, we cut the number of rounds by a factor of $(\delta \log n)^2$.

Theorem 1.4 (constant-round doubly-efficient interactive proofs for $\mathcal{NC}^1$, loosely stated): *Let $\{C_n : \{0,1\}^n \to \{0,1\}\}$ be a sufficiently uniform family of canonical Boolean circuits of fan-in two and logarithmic depth. Then, for every $\delta \in (0,1]$, the set $\{x : C_{|x|}(x) = 1\}$ has a $O(1/\delta^2)$-round interactive proof system in which the verifier runs in time $O(n^{1+o(1)})$, the prescribed prover can be implemented in polynomial-time, and the total communication is $n^{\delta+o(1)}$.*

We stress that Theorem 1.4 does not subsume Theorem 1.1. First, the proof system in Theorem 1.4 uses a larger number of rounds as a function of total communication complexity (i.e., $O(1/\delta^2)$ rather than $O(1/\delta)$ rounds). Second, the uniformity condition in Theorem 1.4 is stronger (cf., Theorem 3.1 and Theorem 2.3).

1.5 Digest and organization

Our constant-round doubly-efficient interactive proof systems (for $\mathcal{AC}^0[2]$ and $\mathcal{NC}^1$) are based on the proof system of Goldwasser, Kalai and Rothblum [8]. Specifically, these proof systems are designed for proving that an input x satisfies a circuit $C_{|x|}$ that is "efficiently constructable" based on $|x|$ only. The proof systems differ in the specific meaning given to the term "efficiently constructable" (see Section 1.2), and they are all pivoted in functions that represent the values of the gates at different layers of the circuit (in its computation on input x).

Typically, the latter functions are too large to be communicated, and their values at specific points cannot be evaluated by the verifier itself (although they are computable in polynomial-time). Still, given x, all these functions are well defined, and they are related by the description of the circuit. The more structured the circuit, the simpler these relations are. In particular, the notions of uniformity defined in Section 1.2 yield very simple relations between the functions that describe the values of gates at adjacent layers.

These relations extend also to low-degree extensions of these functions (which constitute error correcting codes of the explicit description of these functions), and they allow for testing the function that corresponds to layer $i-1$ by using the function that corresponds to layer i. Specifically, the value of the former function at a given point is verified by using the value of the latter function at a few points. Lastly, in contrast to the functions that correspond to higher layers, the function that corresponds to the lowest layer (i.e., the input layer) is known to the verifier (who knows the input x).

In the interactive proof system for $\mathcal{AC}^0[2]$, presented in Section 2 (and establishing Theorem 1.1), a strong notion of uniformity is used to directly relate

functions that describe the values of gates in adjacent layers of a related arithmetic circuit (in a computation on input x). Here we rely on the hypothesis that the original circuit has constant-depth, and capitalize on the fact that we can obtain a corresponding arithmetic circuit that uses multiplication gates of logarithmic fan-in.

In the interactive proof system for $\mathcal{NC}^1$, presented in Section 3 (and establishing Theorem 1.4), an even strong notion of uniformity is used to relate functions that describe the values of gates that are $\delta \log_2 n$ layers apart. Here we rely on the hypothesis that the original circuit has fan-in two and logarithmic depth.

2 The interactive proof system for $\mathcal{AC}^0[2]$

Recall that we consider a sufficiently uniform family of layered circuits $\{C_n\}$ of constant depth $d \in \mathbb{N}$ and unbounded fan-in. For simplicity of our presentation, we work with the adjacency predicate representation, while noting that the handling of other representations can be reduced to it (as detailed in Section 2.5). We also assume, for simplicity, that the circuit has only gates of the `or` and `parity` type, since `and`-gates can be emulated by these. Letting $s = s(n) = \mathrm{poly}(n)$ be a bound on the number of gates in C_n, for each $i \in [d]$, we consider the $n^{o(1)}$-sized formula $\psi_i : [s] \times [s] \to \{0,1\}$ such that $\psi_i(j,k) = 1$ if and only if gate j resides in layer $i-1$ and is fed by the gate k (which resides in layer i). In doing so, we associate $[s]$ with $\{0,1\}^\ell$, where $\ell = \log_2 s$, and view ψ_i as a function over $\{0,1\}^{2\ell}$.

On input $x \in \{0,1\}^n$, we proceed in three steps: First, we reduce the Boolean problem (of verifying that $C_n(x) = 1$) to an Arithmetic problem (of verifying that a related Arithmetic circuit A_n evaluates to 1 on a related input (x,s)). This reduction uses the approximation method and yields constant-depth arithmetic circuits with multiplication gates of logarithmic fan-in. Next, we express the latter problem as a sequence of $O(d)$ functional equations that relate the value of gates at adjacent layers of the circuit A_n. Here we shall use low degree polynomials that extend the ψ_i's, while deriving (succinct representations of) these polynomials from the corresponding Boolean formulas that compute the ψ_i's. Using the fact that all multiplication gates are of small fan-in, it follows that the resulting equations are all of low degree. Last, we present a constant-round doubly-efficient interactive proof system for the verification of this sequence of functional equations. Hence, we obtain a constant-round doubly-efficient interactive proof system for the set $\{x : C_{|x|}(x) = 1\}$.

2.1 Step 1: Approximation by Arithmetic circuits

The first step is a randomized reduction of solving the Boolean problem to solving a corresponding Arithmetic problem. This reduction follows the ideas underlying the approximation method of Razborov [14] and Smolensky [17], while working with the field GF(2) (as [14], rather than with GF(p) for some prime $p > 2$

as [17]). Recall that this reduction replaces every `or`-gate by a $O(\log n)$-way multiplication of parity gates that each computed a random linear combination of the values of the gates that feed the `or`-gate in the Boolean circuit.

When following this scheme, we replace the random choices made at each gate by pseudorandom choices that are generated by a small bias generator [13]; specifically, we use a specific small-bias generator that uses a seed of logarithmic (i.e., $O(\log n)$) length such that its output bits can be succinctly represented by a low-degree function in the bits of the binary extension of the bit's location (e.g., the third construction in [1]).[8] We shall use the same seed to generate all pseudorandom sequences used in the construction, but use different parts of the sequence for each random combination at each gate.

Hence, for a fixed Boolean circuit C_n, on input $x \in \{0,1\}^n$, we randomly reduce the question of whether $C_n(x) = 1$ to the question of whether $A_n^{(\sigma)}(x) = 1$, where $\sigma \in \{0,1\}^{O(\log n)}$ is selected uniformly at random, and $A_n^{(\sigma)}$ is the Arithmetic circuit that results when using σ as the seed for the small-biase generator. Specifically, the choice of σ will be made by the verifier, and we observe that $\Pr_\sigma[A_n^{(\sigma)}(x) = C_n(x)] = 1 - s(n) \cdot \exp(-O(\log n)) = 1 - o(1)$. In the rest of the analysis, we assume that the verifier was not extremely unlucky (in its choice of σ), and so that $A'_n(x) \stackrel{\text{def}}{=} A_n^{(\sigma)}(x) = C_n(x)$ holds. Indeed, we shall fix σ for the rest of this description, and will use the shorthand A'_n.

Let us stop for a moment and take a closer look at A'_n. Recall that each `or`-gate in C_n is essentially replaced by a $O(\log n)$-way multiplication gate that is fed by the inner-product of the values of the original feeding gates and a pseudorandom sequence. Specifically, for $\ell' = O(\log n)$, if the `or`-gate indexed j (at layer $i-1$ of C_n) was fed by gates indexed $k_1, ..., k_{n'}$ (of layer i), then it is replaced in A'_n by an arithmetic sub-circuit that computes the function

$$1 + \prod_{j' \in [\ell']} \left(1 + \sum_{t \in [n']} G'((j-1) \cdot s \cdot \ell' + (j'-1) \cdot s + k_t) \cdot y_{k_t} \right) \tag{1}$$

where y_k represents the output of the gate indexed k (at layer i of C_n), and $G'(k) = G^{(\sigma)}(k)$ is the k^{th} bit in the pseudorandom sequence generated based on the aforementioned fixed seed σ. Note that the ℓ' different linear combinations associated with the same `or`-gate use different portions of the pseudorandom

[8] In the third construction of [1], the seed is viewed as a pair (ζ, r), where $\zeta \in \mathrm{GF}(2^k)$ and $r \in \{0,1\}^k$, and the i^{th} bit in the output is the inner-product (mod 2) of the binary representation of ζ^i and r. Note that computing ζ^i reduces to computing $\prod_{j \geq 0}(i_j \cdot \zeta^{2^j} + (1 - i_j))$, where $(i_{k'-1}, ..., i_0) \in \{0,1\}^{k'}$ is the binary expansion of $i \in [2^{k'}]$ (and $\zeta^2, ..., \zeta^{2^{k'-1}}$ can be precomputed when ζ is fixed). Note that each element of $\mathrm{GF}(2^k)$ is represented as a k-bit long sequence over $\{0,1\} \equiv \mathrm{GF}(2)$, and so multiplication in $\mathrm{GF}(2^k)$ corresponds to k bilinear forms in these representations (and the product $i_j \cdot \zeta^{2^j}$ corresponds to the products of i_j and the bits in the representation of ζ^{2^j}).

sequence. Likewise, different `or`-gates use different portions of the pseudorandom sequence (but this choice is immaterial).[9]

The analysis of the foregoing reduction, which uses related pseudorandom sequences, is almost identical to the analysis of the original reduction (which uses independent random sequences). On the one hand, if $\bigvee_{t\in[n']} y_{k_t} = 0$, then Eq. (1) equals $1 + (1+0)^{\ell'} = 0$. On the other hand, if $\bigvee_{t\in[n']} y_{k_t} = 1$, then, with probability at least $2^{-\ell'} + \epsilon$ (over the choice of σ), it holds that Eq. (1) equals $1 + 0 = 1$, where ϵ denote the bias of the small-biased generator. Indeed, we use the fact that ℓ' disjoint and non-zero linear combinations of the bits of an ϵ-bias generator equal $0^{\ell'}$ with probability at most $2^{-\ell'} + \epsilon$, since this holds for any ℓ' linearly independent combinations. Recall that the aforementined construction of [1] uses a seed of length $O(\log(L/\epsilon))$ in order to generate an ϵ-biased sequence of length L. Hence, we can set $L = \widetilde{O}(s^2)$ and $\epsilon = o(1/s)$, and upper-bound the probability that an approximation-error occured in any of the gate-replacements by using a union bound; that is, this probability is upper-bounded by $s \cdot (2^{-\ell'} + \epsilon) = o(1)$.

Recall that Eq. (1) represents the function computed by a constant-depth sub-circuit that replaces a generic `or`-gate. It will be convenient to think of this function as being computed by a single gate, which we hereafter call an augmented multiplication gate.

We highlight the following features of the Arithmetic circuit A'_n: Its depth is $O(d)$, its size is $O(\log n)^d \cdot s(n)$, it computes a polynomial of degree $O(\log n)^d$, and it has a succinct representation of size $n^{o(1)}$ that can be constructed in time $n^{1+o(1)}$. Furthermore, each of its gates computes a polynomial of degree $O(\log n)^d$. (The forgoing assertions use the fact that, given σ, a circuit computing $G^{(\sigma)} : \{0,1\}^{\log_2(s^2\ell')} \to \{0,1\}$ can be constructed in poly$(|\sigma|)$-time, and that this circuit corresponds to a multilinear function from $\mathrm{GF}(2)^{\log_2(s^2\ell')}$ to $\mathrm{GF}(2)$; see Footnote 8.)

Indeed, as defined above, $A'_n : \mathrm{GF}(2)^n \to \mathrm{GF}(2)$ is an arithmetic circuit over $\mathrm{GF}(2)$, consisting solely of addition and augmented multiplication gates. But we can view A'_n as an arithmetic circuit over $\mathcal{F} = \mathrm{GF}(2^{2\delta \log_2 n})$, and consider its value at $x \in \{0,1\}^n$, which is viewed as an n-long sequence over $\mathcal{F}$. (It suffices to have $|\mathcal{F}| \geq n^{\delta+\Omega(1)}$; on the other hand, we also use $\log_2 |\mathcal{F}| \leq n^{o(1)}$.)

2.2 Step 2: Relating the values of layers in the computation

A key idea of Goldwasser, Kalai and Rothblum [8] consists of representing the values of the gates at various levels of the circuit by functions, and relating these functions by functions that represent the structure of the circuit. (These functions are first viewed as functions from $[s]$ to $\{0,1\}$, and then as ℓ-variant

[9] This is the case since we bound the approximation error of A'_n by employing a union bound to the errors that may occur in the various gates, and these hold regardless of the dependency between these error evants.

functions from $\{0,1\}^\ell$ to $\{0,1\}$, which serves as basis for considering their low degree extensions over larger fields (i.e., $\mathcal{F}$ as above).)[10]

In our context, we use the functions $\alpha_d, ..., \alpha_0 : [s] \to \{0,1\}$ such that $\alpha_{i-1}(j)$ represents the value of gate j (at layer $i-1$) in a computation of $A'_n(x)$. We then relate their values by referring to ψ_i and to the functionality of the gates in layer i. Recall that $\psi_i(j,k) = 1$ if gate j (of layer $i-1$) is fed by gate k (of layer i). In the case of an addition gate (i.e., a layer of addition gates), we have

$$\alpha_{i-1}(j) = \sum_{k \in [s]} \psi_i(j,k) \cdot \alpha_i(k). \tag{2}$$

Hence, Eq. (2) can be viewed as relating functions that range over $[s]$ by using a function that ranges over $[s]^2$. In the case of an augmented multiplication gate (as represented by Eq. (1)), we have

$$\alpha_{i-1}(j) = 1 + \prod_{j' \in [\ell']} \left(1 + \sum_{k \in [s]} G'((j-1) \cdot s \cdot \ell' + (j'-1) \cdot s + k) \cdot \psi_i(j,k) \cdot \alpha_i(k) \right) \tag{3}$$

where (as before) $G'(k)$ represents the k^{th} bit in the output of the generator on the fixed seed. Assuming, without loss of generality, that $\ell' > 2\ell + \log_2 \ell'$ (equiv., $2^{\ell'} > s^2 \cdot \ell'$), we view Eq. (3) as relating functions that range over $[s]$ by using functions that range over $[2^{\ell'}] \supset [s]^2 \cup [s]^2 \times [\ell']$.

The next step is viewing all functions as functions over binary strings rather than over natural numbers; that is, we associate $[s]$ with $\{0,1\}^\ell$, and $[2^{\ell'}]$ with $\{0,1\}^{\ell'}$. Furthermore, we consider the arithmetic formula $\widehat{\psi}_i : \mathcal{F}^{\ell+\ell} \to \mathcal{F}$ that is derived from $\psi_i : \{0,1\}^{\ell+\ell} \to \{0,1\}$ in the obvious manner (i.e., replacing `and`-gates by multiplication gates and negation gates by gates that add the constant 1). Recalling that ψ_i is a formula of size $n^{o(1)}$, it follows that $\widehat{\psi}_i$ computes a polynomial of degree $n^{o(1)}$. Hence, Eq. (2) is replaced by

$$\alpha_{i-1}(j) = \sum_{k \in \{0,1\}^\ell} \widehat{\psi}_i(j,k) \cdot \alpha_i(k), \tag{4}$$

where $j \in \{0,1\}^\ell$. Hence, the functions $\alpha_{i-1} : \{0,1\}^\ell \to \{0,1\}$ and $\alpha_i : \{0,1\}^\ell \to \{0,1\}$ are related by an equation that uses a low degree polynomial (i.e., $\widehat{\psi}_i$). The same consideration can be applied to Eq. (3), when recalling that $G' : [2^{\ell'}] \to \{0,1\}$ can be written as an explicit low-degree polynomial by using functions that range over $\{0,1\}^{\ell'} \equiv [2^{\ell'}]$. Specifically, the corresponding low degree polynomial

[10] Jumping ahead, we stress that the relation between these functions will be checked by the interactive proof system presented in Section 2.3. This will be done by having the verify ask the prover to provide the values of these functions in few places, while relying on the fact that these functions can be evaluated in polynomial-time. Note that these functions are too large to be communicated to the verifier (see analogous discussion in Section 3.1.)

is $\widehat{G'} : \mathcal{F}^{\ell'} \to \mathcal{F}$ such that $\widehat{G'}(z_{\ell'}, ..., z_1)$ is a specific linear combination (i.e., r) of the bits of the field element $\prod_{j \in [\ell']}(z_j \cdot \tau_j + (1 - z_j))$, where r as well as the τ_j's are precomputed based on the fixed seed of the small-biased generator G (see Footnote 8).[11] Hence, we get

$$\alpha_{i-1}(j) = 1 + \prod_{j' \in \{0,1\}^{\log_2 \ell'}} \left(1 + \sum_{k \in \{0,1\}^{\ell}} \widehat{G'}(j, j', k) \cdot \widehat{\psi}_i(z, k) \cdot \alpha_i(k) \right) \quad (5)$$

where $j \in \{0,1\}^{\ell}$.

At this point, the standard approach taken in [8] (and followed also in Section 3) is to extend Eq. (4)-(5) to any $j \in \mathcal{F}^{\ell}$ by using a low-degree extension (see also Eq. (8)). This is redundent in the case of Eq. (4)-(5), since the r.h.s. of these equations is well defined also when $j \in \mathcal{F}^{\ell}$. Hence, we can replace Eq. (4) by

$$\widehat{\alpha}_{i-1}(z) = \sum_{k \in H^m} \widehat{\psi}_i(z, k) \cdot \alpha_i(k), \quad (6)$$

where $z \in \mathcal{F}^{\ell}$. Assuming that α_i is also extended to a low-degree polynomial, denoted $\widehat{\alpha}_i$, we can replace $\alpha_i(k)$ by $\widehat{\alpha}_i(k)$. In this case, the degree of $\widehat{\alpha}_{i-1}$ equal the sum of the degrees of $\widehat{\psi}_i$ and $\widehat{\alpha}_i$, where the degree of $\widehat{\psi}_i$ is $n^{o(1)}$. In the case of Eq. (3), we get, for every $z \in \mathcal{F}^{\ell}$

$$\widehat{\alpha}_{i-1}(z) = 1 + \prod_{j' \in \{0,1\}^{\log_2 \ell'}} \left(1 + \sum_{k \in \{0,1\}^{\ell}} \widehat{G'}(z, j', k) \cdot \widehat{\psi}_i(z, k) \cdot \widehat{\alpha}_i(k) \right), \quad (7)$$

In this case the degree of $\widehat{\alpha}_{i-1}$ equal ℓ' times the sum of the degrees of $\widehat{\psi}_i$, $\widehat{G'}$ and $\widehat{\alpha}_i$, where the degree of $\widehat{G'}$ is ℓ' (and the degree of $\widehat{\psi}_i$ is $n^{o(1)}$).

Note, however, that the foregoing can not be applied to α_d, which is supposed to encode the input x to A'_n. This function is well-defined only over $[s] \equiv \{0,1\}^{\ell}$; specifically, recall that $\alpha_d(j) = x_j$ for $j \in [n]$, whereas $\alpha_d(j) = j \bmod 2$ for $j \in \{n+1, n+2\}$, and $\alpha_d(j) = 0$ for $j \in [s] \setminus [n+2]$.[12] Hence, we augment

[11] Here we assume that the length of the seed is $2\ell'$, which is justified by the fact that we can afford any $\ell' = O(\log n)$. Recall that, for $(i_{\ell'}, ..., i_1) \in \{0,1\}^{\ell'}$, if $\tau_j = \zeta^{2^{j-1}}$, then $\prod_{j \in [\ell']}(i_j \cdot \tau_j + (1 - i_j)) = \zeta^i$ such that $i = \sum_{j \in [\ell']} i_j \cdot 2^{j-1}$. (Recall the product is over $\mathrm{GF}(2^{\ell'})$, but each multiplication over $\mathrm{GF}(2^{\ell'})$ is emulated by bilinear forms in the bits of the representations of the $\mathrm{GF}(2^{\ell'})$-elements.) In this case, $\widehat{G'}(i_{\ell'}, ..., i_1)$ equals the inner product (mod 2) of r and the binary representation of ζ^i, where $(\zeta, r) = \sigma$ is the seed of the generator.

[12] Recall that we need to provide the circuit with the constants 1 and 0, hence we set $\{\alpha_d(n+1), \alpha_d(n+2)\} = \{0,1\}$. The setting of $\alpha_d(j) = 0$ for $j \in [s] \setminus [n+2]$ is used in order to facilitate the evaluation of r.h.s. of Eq. (8), as discussed below and used in Step 3; that is, this setting ensures that, for every $u \in \mathcal{F}^{\ell}$, it holds that

the foregoing definitions by postulating that $\widehat{\alpha}_d$ is a low-degree extension of the values of α_d at $\{0,1\}^\ell$; that is, for $z \in \mathcal{F}^\ell$, we have

$$\widehat{\alpha}_d(z) = \sum_{k \in \{0,1\}^\ell} \mathtt{EQ}(z,k) \cdot \alpha_d(k), \tag{8}$$

where $\mathtt{EQ}$ is the bilinear polynomial that extends the function that tests equality over $\{0,1\}^\ell$ (e.g., $\mathtt{EQ}(\sigma_1 \cdots \sigma_\ell, \tau_1 \cdots \tau_\ell) = \prod_{i \in [\ell]}(\sigma_i\tau_i + (1-\sigma_i)(1-\tau_i))$). Note that r.h.s. of Eq. (8) depends only on $n+2$ terms, since $\alpha_d(j) = 0$ for $j \notin [n+2]$.

Lastly, we wish to replace summation over $\{0,1\}^\ell$ by summation over H^m, where $|H| = n^\delta$ and $m = \frac{\ell}{\delta \log n} = O(1/\delta)$. Towards this end, we introduce a 1-1 mapping $\mu : H \to \{0,1\}^{\ell''}$, where $\ell'' = \delta \log n = \ell/m$, such that $\mu(h)$ returns the ℓ''-bit long binary representation of $h \in H$. Next, we extended $\mu : H \to \{0,1\}^{\ell''}$ to an ℓ''-long sequence of univariate polynomials of degree $|H|-1$ over $\mathcal{F}$; that is, $\mu : \mathcal{F} \to \mathcal{F}^{\ell''}$ is defined as $\mu(z) = (\mu_{\ell''}(z), ..., \mu_i(z))$ such that $\mu_i(z) = \sum_{h \in H} \prod_{h' \in H \setminus \{h\}} \frac{z-h'}{h-h'} \cdot \mathtt{bin}_i(h)$, where $\mathtt{bin}_i(h)$ is the i^{th} bit in the binary representation of $h \in H \equiv \{0,1\}^{\ell''}$. The next step is extending μ to m-long sequences of such sequences; that is, we use $\widehat{\mu} : \mathcal{F}^m \to (\mathcal{F}^{\ell''})^m$ such that for every $h = (h_1, ..., h_m) \in H^m$ it holds that $\widehat{\mu}(h) = (\mu(h_1), ..., \mu(h_m)) \in \{0,1\}^{m \cdot \ell''}$, whereas $m\ell'' = \ell$. Finally, we redefine the $\widehat{\alpha}_i$'s so that they range over $\mathcal{F}^m$ (rather than over $\mathcal{F}^\ell$). Starting with Eq. (8), we have

$$\widehat{\alpha}_d(z) = \sum_{k \in H^m} \mathtt{EQ}(\widehat{\mu}(z), \widehat{\mu}(k)) \cdot \alpha_d(\widehat{\mu}(k)), \tag{9}$$

where $z \in \mathcal{F}^m$. (Alternatively, we could have defined α_d over H^m, and presented a direct equality-testing polynomial for sequences over H^m.) Turning to Eq. (6), we replace it by

$$\widehat{\alpha}_{i-1}(z) = \sum_{k \in H^m} \widehat{\psi}_i(\widehat{\mu}(z), \widehat{\mu}(k)) \cdot \widehat{\alpha}_i(k) \tag{10}$$

where again $z \in \mathcal{F}^m$. Lastly, Eq. (7) is replaced by

$$\widehat{\alpha}_{i-1}(z) = 1 + \prod_{j' \in \{0,1\}^{\log_2 \ell'}} \left(1 + \sum_{k \in H^m} \widehat{G'}(\widehat{\mu}(z), \widehat{\mu}(j'), \widehat{\mu}(k)) \cdot \widehat{\psi}_i(\widehat{\mu}(z), \widehat{\mu}(k)) \cdot \widehat{\alpha}_i(k)\right) \tag{11}$$

where we assume that $\{0,1\} \subset H$. Denoting the degree of a polynomial p by $\mathtt{deg}(p)$, we have $\mathtt{deg}(\widehat{\alpha}_d) = \mathtt{deg}(\mathtt{EQ}) \cdot \mathtt{deg}(\widehat{\mu}) < \ell \cdot |H|$. For i that is an addition layer (i.e., Eq. (10)), we have $\mathtt{deg}(\widehat{\alpha}_{i-1}) = \mathtt{deg}(\widehat{\psi}_i) \cdot \mathtt{deg}(\widehat{\mu}) + \mathtt{deg}(\widehat{\alpha}_i) < n^{o(1)} \cdot |H| +$

$\sum_{k \in \{0,1\}^\ell} \mathtt{EQ}(u,k) \cdot \alpha_d(k)$ equals $\sum_{k \in I} \mathtt{EQ}(u,k) \cdot \alpha_d(k)$, where $I \subset \{0,1\}^\ell$ corresponds to $[n+2]$. Alternatively, we could have used the setting $\alpha_d(j) = 1$ for $j \in [s] \setminus [n]$, and rely on the fact that $\sum_{k \in \{0,1\}^\ell} \mathtt{EQ}(u,k)$ equals 1.

$\mathtt{deg}(\widehat{\alpha}_i)$. Lastly, for i that is an augmented multiplication layer (i.e., Eq. (11)), we have

$$\begin{aligned}\mathtt{deg}(\widehat{\alpha}_{i-1}) &< \ell' \cdot \left(\mathtt{deg}(\widehat{G'}) \cdot |H| + \mathtt{deg}(\widehat{\psi}_i) \cdot |H| + \mathtt{deg}(\widehat{\alpha}_i)\right) \\ &= \ell' \cdot n^{o(1)} \cdot |H| + \ell' \cdot \mathtt{deg}(\widehat{\alpha}_i).\end{aligned}$$

Hence, $\mathtt{deg}(\widehat{\alpha}_0) < (O(\log n)^d + n^{o(1)}) \cdot |H| = n^{\delta+o(1)}$.

2.3 Step 3: Obtaining an interactive proof system (with imperfect completeness)

On input $x \in \{0,1\}^n$, the verifier selects uniformly $\sigma \in \{0,1\}^{O(\log n)}$, and sends σ to the prover. The prover now attempts to prove that $A'_n(x) \stackrel{\text{def}}{=} A_n^{(\sigma)}(x) = 1$, where a succinct representation of A'_n (which has size $n^{o(1)}$) can be constructed in time $n^{1+o(1)}$. The initial claim is re-interpreted as $\widehat{\alpha}_0(\mu^{-1}(1^\ell)) = 1$, where $\mu^{-1}(1^\ell) = (\mu^{-1}(1^{\ell/m}), ..., \mu^{-1}(1^{\ell/m})) \in H^m \subset \mathcal{F}^m$. (Recall that $\widehat{\alpha}_i : \mathcal{F}^m \to \mathcal{F}$ for every i, and that $\mu : H \to \{0,1\}^{\ell/m}$ is a bijection).

The parties proceed in $O(d)$ steps such that the i^{th} step starts with a claim regarding the value of $\widehat{\alpha}_{i-1}$ at few points, and ends with a claim regarding the value of $\widehat{\alpha}_i$ at few points, where the said number of points may increase by at most a logarithmic factor. We distinguish between the case that the current layer (i.e., $i-1$) is of addition gates and the case that it is of augmented multiplication gates.

Handling a layer of addition gates: (Recall that these gates are supposed to satisfy Eq. (10).) For each claim of the form $\widehat{\alpha}_{i-1}(u) = v$, where $u \in \mathcal{F}^m$ and $v \in \mathcal{F}$ are known, we invoke the Sum-Check protocol on the r.h.s. of Eq. (10). The execution of this (m-round) protocol results in a claim regarding the value $\widehat{\psi}_i(\widehat{\mu}(u), \widehat{\mu}(r)) \cdot \widehat{\alpha}_i(r)$ for a random $r \in \mathcal{F}^m$ selected via the execution. Since the verifier can evaluate $\widehat{\mu}$ and $\widehat{\psi}_i$, it is left with a claim regarding the value of $\widehat{\alpha}_i$ at one point.

Recall that the Sum-Check protocol proceeds in $m = O(1/\delta)$ rounds, where in each round the prover sends the value of the relevant univariate polynomial. This is a polynomial of degree $|H| \cdot n^{o(1)} = n^{\delta+o(1)}$, where the degree bound is due to the composition of the polynomials $\widehat{\mu}$ and $\widehat{\psi}_i$ (and to the degree of $\widehat{\alpha}_i$).[13]

Handling a layer of augmented multiplication gates: (Recall that these gates are supposed to satisfy Eq. (11).) For each claim of the form $\widehat{\alpha}_{i-1}(u) = v$, where u and v are known, we let the prover send the values $(v_1, ..., v_{\ell'})$ such that

$$v_{j'} \stackrel{\text{def}}{=} \sum_{k \in H^m} \widehat{G'}(\widehat{\mu}(u), \widehat{\mu}(j'), \widehat{\mu}(k)) \cdot \widehat{\psi}_i(\widehat{\mu}(u), \widehat{\mu}(k)) \cdot \widehat{\alpha}_i(k). \tag{12}$$

[13] Recall that the degree of $\widehat{\psi}_i$ is upper bounded by $n^{o(1)}$, since it is obtained by arithmetizing the formula ψ_i which has size $n^{o(1)}$, whereas $\widehat{\mu}$ has degree $|H| - 1$. As for the degree of $\widehat{\alpha}_i$ – see the end of Section 2.2.

The verifier checks that $v = 1+\prod_{j' \in [\ell']}(1+v_{j'})$ holds, and the parties invoke the ℓ' parallel executions of Sum-Check protocol in order to to verify that each $v_{j'}$ matches the r.h.s. of Eq. (12). The execution indexed by $j' \in [\ell']$ results in a claim regarding the value $\widehat{G'}(\widehat{\mu}(u), \widehat{\mu}(j'), \widehat{\mu}(r)) \cdot \widehat{\psi}_i(\widehat{\mu}(u), \widehat{\mu}(r)) \cdot \widehat{\alpha}_i(r)$ for a random $r \in \mathcal{F}^m$ selected via the execution. Since the verifier can evaluate $\widehat{\mu}, \widehat{\psi}_i$ and $\widehat{G'}$, it is left with $\ell' = O(\log n)$ claims, each regarding the value of $\widehat{\alpha}_i$ at one point.[14]

After $O(d)$ steps, the verifier is left with polylogarithmically (i.e., $O(\log n)^d$) many claims, where each claim refers to the value of $\widehat{\alpha}_d$ at a single point $u \in \mathcal{F}^m$. Such a claim can be checked by the verifier itself using Eq. (9).

Note that a straightforward computation of the r.h.s. of Eq. (9) calls for summing-up $|H^m| = 2^\ell = \text{poly}(n)$ terms, which the verifier cannot afford. However, all but $n+2$ of these terms (of the form $\texttt{EQ}(\widehat{\mu}(u), \widehat{\mu}(k)) \cdot \alpha_d(\widehat{\mu}(k))$), are identically zero, and so the verifier needs to compute only $n+2$ terms. This is the case because $\alpha_d(k) = 0$ for every $k \in [s] \setminus [n+2]$ (whereas $\alpha_d(k) = x_k$ for every $k \in [n]$ and $\{\alpha_d(n+1), \alpha_d(d+2)\} = \{0.1\}$). Hence, per each point $u \in \mathcal{F}^m$, computing $\widehat{\alpha}_d(u)$ reduces to evaluating $\texttt{EQ}(\widehat{\mu}(u), \widehat{\mu}(k)) \cdot \alpha_d(\widehat{\mu}(k))$ at $n+2$ points (only); that is, letting I denote the subset of $H^m \equiv [2^\ell]$ that correspond to $[n+2]$, the verifier just computes $\sum_{k \in I} \texttt{EQ}(\widehat{\mu}(u), \widehat{\mu}(k)) \cdot \alpha_d(\widehat{\mu}(k))$.

Analysis of the forgoing interactive proof system. We first observe that the complexities of the foregoing protocol are as stated in Theorem 1.1. Specifically, the protocol proceeds in $O(d)$ steps and in each step a Sum-Check protocol is invoked on a sum that ranges over H^m, where $m = O(1/\delta)$ and $|H| = n^\delta$. Since the relevant polynomial is of degree $n^{\delta+o(1)}$, the total (m-round) communication is of this order.[15] The total number of rounds is $O(d \cdot m) = O(d \log_{n^\delta} s(n)) = O(d \cdot c/\delta)$, where $s(n) = n^c$. The verification time is dominated by the final check (i.e., evaluating $\widehat{\alpha}_d$ on $\text{poly}(\log n)$ points), which runs in time $\widetilde{O}(n) \cdot n^{o(1)} = O(n^{1+o(1)})$. The complexity of the prescribed prover is dominated by its operation in the Sum-Check protocol, which can be implemented in time $|H|^m \cdot n^{o(1)} = 2^\ell \cdot n^{o(1)} = s(n)^{1+o(1)}$. Next, we show that this protocol constitutes an interactive proof system (with imprefect completeness) for $\{x : C_{|x|}(x) = 1\}$.

Claim 2.1 (imperfect completeness): *If $C_n(x) = 1$ and the prover follows the presecribed strategy, then the verifier accepts with probability $1 - o(1)$.*

Proof: The probability that the value of an `or`-gate, under a fixed setting of its input wires, is correctly emulated by the multiplication of ℓ' random linear combinations of these wires is at least $1 - 2^{-\ell'}$, where in case all wires feed 0 the

[14] Indeed, we could afford letting the verifier use the same random choices in all ℓ' parallel executions, which would result in leaving it with a single claim regarding the value of $\widehat{\alpha}_i$ at one point (i.e., r).

[15] This dominates the length of the initial verifier-message $\sigma \in \{0,1\}^{O(\log n)}$.

emulation is always correct. The same holds (approximately) when the random linear combinations are replaced by inner products with a small biased sequence; specifically, if the sequence is ϵ-biased, then the emulation is correct with probability at least $1 - 2^{-\ell'} + \epsilon$. Using $\ell' = 2\log_2 s(n) = O(\log n)$ and $\epsilon = 2^{-\ell'}$, and employing a union bound, it follows that with probability $1 - o(1)$ over the choice of the random seed $\sigma \in \{0,1\}^{O(\log n)}$, it holds that $A_n^{(\sigma)}(x) = C_n(x)$. Observing that the verifier always accepts when $A_n^{(\sigma)}(x) = 1$ (and the prover follows the prescribed strategy), the claim follows. ∎

Claim 2.2 (soundness): *If $C_n(x) = 0$, then, no matter what strategy the prover employs, the verifier accepts with probability at most $o(1)$.*

Proof: As shown in the proof of Claim 2.1, with probability $1 - o(1)$ it holds that $A_n^{(\sigma)}(x) = C_n(x)$. Recalling that the soundness error of the Sum-Check protocol is proportional to the ratio of the degree of the polynomial over the size of the field, it follows that the prover can fool the verifier into accepting a wrong value of $A_n^{(\sigma)}(x)$ with proability $O(dm)\cdot|H|\cdot n^{o(1)}/|\mathcal{F}| = n^{\delta+o(1)-2\delta} = o(1)$, since $|\mathcal{F}| = n^{2\delta}$. The claim follows. ∎

2.4 Getting rid of the completeness error

Claims 2.1 and 2.2 assert that the foregoing protocol constitutes a proof system for $\{x : C_{|x|}(x) = 1\}$, but this proof system carries a completeness error (see Claim 2.1). Recalling that this error is only due to the (unlikely) case that $A_n^{(\sigma)}(x) \neq C_n(x)$, the begging fix is to have the prover prove to the verifier that this case has occurred (with respect to the random seed σ chosen by the verifier). Specifically, the (unlikely) case that $A_n^{(\sigma)}(x) \neq C_n(x)$ may occur only when at least one `or`-gate of C_n is badly emulated by $A_n^{(\sigma)}$; that is, the value of this gate is 1 in the computation of $C_n(x)$ whereas the corresponding (augmented multiplication) gate in $A_n^{(\sigma)}(x)$ evaluates to 0. This means that at least one of the gates (in $A_n^{(\sigma)}$) that correspond to the children of the `or`-gate in C_n evaluates to 1, whereas the gate (in $A_n^{(\sigma)}$) that corresponds to the `or`-gate (of C_n) evaluates to 0. So all that the prover needs to do is point out these two gates in $A_n^{(\sigma)}$, and prove that their values are as stated. Hence, we regain perfect completeness, whereas the soundness claim remains valid (since in order to cheat the prover has to prove a false claim regarding the value of a gate in $A_n^{(\sigma)}$). Thus, we obtain:

Theorem 2.3 (Theorem 1.1, restated): *For constants $c, d \in \mathbb{N}$, let $\{C_n : \{0,1\}^n \to \{0,1\}\}$ be a family of layered Boolean circuits with unbounded fan-in* `or`, `and`, *and* `parity` *gates such that C_n has size at most n^c and depth d. Suppose that C_n can be described by an adjacency predicate that is computable by a $n^{o(1)}$-size formula that can be constructed in $n^{1+o(1)}$-time. Then, for every $\delta \in (0,1]$, the set $\{x : C_{|x|}(x) = 1\}$ has a $O(cd/\delta)$-round interactive proof system of perfect completeness in which the verifier runs in time $O(n^{1+o(1)})$, the prescribed prover can be implemented in time $O(n^{c+o(1)})$, and the total communication is $n^{\delta+o(1)}$.*

Note that the foregoing adjacency predicate refers to gates of C_n, which are identified by ℓ-bit long strings, where $\ell = O(\log n)$. Thus, the uniformity condition postulates that this predicate can be computed by a formula of size $\exp(o(\ell))$ (equiv., by a bounded fan-in circuit of depth $o(\ell)$) that can be constructed in time $\exp(\ell/O(1))$.

2.5 Using the other two succinct representations

The foregoing presentation refers to Bollean circuits C_n that are succinctly represented by their adjacency predicates. Specifically, we referred to the adjacency predicates $\psi_i : \{0,1\}^{2\ell} \to \{0,1\}$, which were extended to $\widehat{\psi}_i : \mathcal{F}^{2\ell} \to \mathcal{F}$. In this section we show that the presentation can be adapted to the other two succinct representations of circuits discussed in Section 1.2.

From incidence functions to adjacency predicate. Suppose that the circuit C_n is represented by incidence functions of the form $\phi_i : [s] \times [s] \to [s] \cup \{0\}$, which we view as $\phi_i : \{0,1\}^{2\ell} \to \{0,1\}^{\ell+1}$, where $[s] \equiv \{0,1\}^\ell$ is identified with $\{1\sigma : \sigma \in \{0,1\}^\ell\}$ and $0 \equiv 0^{\ell+1}$. Using a multi-linear extenstion of ϕ_i, denoted $\widehat{\phi}_i : \mathcal{F}^{2\ell} \to \mathcal{F}^{\ell+1}$, for any $j,k \in [s] \equiv \{0,1\}^\ell$, we replace the adjacency value $\widehat{\psi}_i(j,k)$ by the expression $\sum_{p\in\{0,1\}^\ell} \mathtt{EQ}(\widehat{\phi}_i(j,p), 1k)$, since the latter expression equals 1 if and only if $\widehat{\psi}_i(j,p) = 1k$ for a unique $p \in [s]$ (which means that k feeds j). Actually, $\widehat{\psi}_i(j,k)$ is replaced by $\sum_{p\in H^m} \mathtt{EQ}(\widehat{\phi}_i(j,\widehat{\mu}(p)), 1k)$. This means that, in the invocations of the Sum-Check protocol, the relevant summations are over H^{2m} rather than over H^m.

Handling canonical circuits. In this case, the s-sized circuit of depth d has the form of a w-ary tree of depth d such that $w = s^{1/d}$, and the input assignment is represented by a function of the form $\pi : \{0,1\}^\ell \to [n+2]$. Hence, we effectively refer to the adjacency predicate $\psi_i : [w]^d \times [w]^d \to \{0,1\}$ such that $\psi_i(j_1 \cdots j_d, k_1 \cdots k_d) = 1$ if and only if $j_1 \cdots j_{i-1} j_{i+1} \cdots j_d = k_1 \cdots k_{i-1} k_{i+1} \cdots k_d$ (or rather $\psi_i : [w]^{i-1} \times [w]^i \to \{0,1\}$ such that $\psi_i(j_1 \cdots j_{i-1}, k_1 \cdots k_i) = 1$ if and only if $j_1 \cdots j_{i-1} = k_1 \cdots k_{i-1}$).[16] In addition, instead of Eq. (8) (or rather Eq. (9)), letting I be a subset of H^m that corresponds to $[n+2]$, for $z \in \mathcal{F}^m$, we have

$$\widehat{\alpha}_d(z) = \sum_{k\in H^m} \mathtt{EQ}(\widehat{\mu}(z), \widehat{\mu}(k)) \cdot \sum_{p\in I} \mathtt{EQ}(p, \widehat{\pi}(\widehat{\mu}(k))) \cdot x_p \tag{13}$$

where $x_p = p \bmod 2$ for $p \in \{n+1, n+2\}$ and $\widehat{\pi}$ is polynomial that is obtained by transforming the Boolean formula that computes π to a corresponding arithmetic formula. The outer sum (in Eq. (13), along with $\mathtt{EQ}(\widehat{\mu}(z), \widehat{\mu}(k))$) implements a selector of one of the leaves in the canonical circuit (i.e., if $z \in H^m$, then leaf z is selected). In contrast, the inner sum (along with $\mathtt{EQ}(p, \widehat{\pi}(\widehat{\mu}(k)))$) implements a selector of a variable (i.e., x_i for $i \in [n]$) or the constants 0 and 1

[16] Indeed, we can replace Eq. (2) by $\alpha_{i-1}(j_1 \cdots j_d) = \sum_{k_i\in[w]} \alpha_i(j_1 \cdots j_{i-1} k_i j_{i+1} \cdots j_d)$ (or rather by $\alpha_{i-1}(j_1 \cdots j_{i-1}) = \sum_{k_i\in[w]} \alpha_i(j_1 \cdots j_{i-1} k_i)$), and ditto for Eq. (3).

(i.e., $\{x_{n+1}, x_{n+2}\} = \{0,1\}$ by definition). Hence, for $k \in H^m$, it holds that $\widehat{\alpha}_d(k) = \sum_{p \in I} \mathtt{EQ}(p, \widehat{\pi}(\widehat{\mu}(k))) \cdot x_p$, which equals $x_{\widehat{\pi}(\widehat{\mu}(k)))}$, since $\widehat{\pi}(k') \in [n+2]$ for every $k' \in \{0,1\}^\ell$.

Recall that once the $O(d)$ iterations are completed, the verifier is left with the verification of polylogarithmically many claims, where each claim refers to the value of $\widehat{\alpha}_d$ at a single point $u \in \mathcal{F}^m$. Here we cannot afford having the verifier evaluate $\widehat{\alpha}_d$ at u by itself (since this requires evaluating the $|H|^m = s$ terms of the outer sum). Instead, we instruct the parties to run the Sum-Check protocol on Eq. (13), and the verifier is left with a claim referring to the value of $\mathtt{EQ}(\widehat{\mu}(u), \widehat{\mu}(r)) \cdot \sum_{p \in I} \mathtt{EQ}(p, \widehat{\pi}(\widehat{\mu}(r))) \cdot x_p$ at a random point $r \in \mathcal{F}^m$, which can be verified in time $|I| \cdot n^{o(1)} = n^{1+o(1)}$.

3 The interactive proof system for $\mathcal{NC}^1$

In this section we prove the following result.

Theorem 3.1 (Theorem 1.4, restated): *For a logarithmic function $d : \mathbb{N} \to \mathbb{N}$, let $\{C_n : \{0,1\}^n \to \{0,1\}\}$ be a family of canonical Boolean circuits of fan-in two and depth d. Suppose that the input assignment of C_n can be computed by a $n^{o(1)}$-size formula that can be constructed in $n^{1+o(1)}$-time. Then, for every $\delta \in (0,1]$, the set $\{x : C_{|x|}(x) = 1\}$ has a $O(d(n)/\delta \log n)^2$-round interactive proof system of perfect completeness in which the verifier runs in time $O(n^{1+o(1)})$, the prescribed prover can be implemented in polynomial-time, and the total communication is $n^{\delta+o(1)}$.*

We leave open the question of whether the round complexity can be reduced to $O(\delta^{-1} \cdot (d(n)/\log n)^2)$, meeting the bound in Theorem 2.3.

3.1 Overview

The construction generalizes and somewhat simplifies the proof systems constructed by Goldwasser, Kalai, and Rothblum [8]. The simplification is due to working with canonical circuits rather than with general (log-space) uniform circuits as in [8], whereas the generalization allows us to reduce the round complexity of [8] by a log-squared factor. Specifically, the canonical form of the circuit allows us to relate the values of layers in the circuit that are at distance $\delta \log_2 n$ apart, whereas [8] relate values at adjacent layers (only). In addition, we use a version of the sum-check protocol that handles summations over an alphabet of size n^δ (rather than over the alphabet $\{0,1\}$).

Fixing a constant $\delta \in (0,1)$, let $\ell' = \delta \log_2 n$. The core of the proof system asserted in Theorem 3.1 is an iterative process in which a claim about the values of the gates that are at layer $(i-1) \cdot \ell'$ is reduced to a claim about the values of the gates at layer $i \cdot \ell'$. We stress that each of these claims refers to the values of the polynomially many gates at a specific layer of the circuit $C_{|x|}$ during the computation on input x, but these poly($|x|$) values are not communicated

explicitly but rather only referred to. Nevertheless, in $t = d(|x|)/\ell'$ iterations, the claim regarding the value of the output gate (i.e., the value $C_{|x|}(x)$) is reduced to a claim regarding the values of the bits of the input x, whereas the latter claim (which refers to x itself) can be verified in almost linear time.

Each of the aforementioned claims regarding the values of the gates at layer $i \cdot \ell'$, where $i \in \{0, 1, ..., t\}$, is actually a claim about the value of a specified location in the corresponding encoding of the (string that describing all the) gate-values at layer $i \cdot \ell'$. Specifically, the encoding used is the low degree extension of the said string (viewed as a function), and the claims are claims about the evaluations of these polynomials at specific points.

The different codewords (or polynomials) are related via the structure of the circuit $C_{|x|}$, which is the case of canonical circuit is straightforward to implement (avoiding a main source of technical difficulty in [8] (see also [4])). Indeed, this reduces a claim regarding one value in the encoding of layer $(i-1)\cdot\ell'$ to $2^{\ell'} = n^{\delta}$ analogous claims regarding layer $i \cdot \ell'$, but (as in [8]) "batch verification" is possible, reducing these $2^{\ell'}$ claims to a single claim.

3.2 The actual construction

For simplicity (and w.l.o.g.), we assume that C_n contains only NAND-gates of (fan-in two), where $\mathtt{NAND}(a, b) = \neg(a \wedge b)$. Viewing this gate as operating in a finite field that contains $\{0, 1\}$, we have $\mathtt{NAND}(a, b) = 1 - (a \cdot b)$ for $a, b \in \{0, 1\}$. The function computed by tree of depth i of such gates is given by

$$\mathtt{NAND}_i(b_1, ..., b_{2^i}) = 1 - (\mathtt{NAND}_{i-1}(b_1, ..., b_{2^{i-1}}) \cdot \mathtt{NAND}_{i-1}(b_{2^{i-1}+1}, ..., b_{2^i})), \quad (14)$$

where $b_1, ..., b_{2^i} \in \{0, 1\}$ are the values at its leaves and $\mathtt{NAND}_0(b) = b$; indeed, $\mathtt{NAND}_1 = \mathtt{NAND}$.

For sake of simplifying the notation, we fictitiously augment the circuit with gates that are fed by no gate (and feed no gate), where (by convention) gates that are fed nothing always evaluate to 0, so that all layers of the circuits have the same number of gates. Hence, we present the circuit as having $d(n) + 1$ layers of gates such that each layer has exactly $k(n) = 2^{d(n)} = \mathrm{poly}(n)$ gates. As usual, the gates at layer i are only fed by gates at layer $i+1$, and the leaves (at layer $d(n)$) are input-variables or constants. Recall that the latter assignment is represented by the function $\pi : \{0, 1\}^{\ell} \to [n + 2]$, where $\ell = d(n)$ and $[k(n)] \equiv \{0, 1\}^{\ell}$, such that the j^{th} leaf is fed the variable $x_{\pi(j)}$ if $\pi(j) \in [n]$ (and the constant $\pi(j)$ mod n otherwise). The output is produced at the first gate of layer zero.

The high level protocol. On input $x \in \{0, 1\}^n$, the prescribed prover computes the values of all layers. Letting $d = d(n)$ and $k = k(n)$, we denote the values at the i^{th} layer by $\alpha_i \in \{0, 1\}^k$; in particular, $\alpha_0 = C_n(x)0^{k-1}$ and α_d is the sequence of values given by $x_{\pi(0^{\ell})}, ..., x_{\pi(1^{\ell})}$, where $x_j = j$ mod 2 for $j \in \{n+1, n+2\}$. For a sufficiently large finite field, denoted $\mathcal{F}$, consider an arbitrary fixed set $H \subset \mathcal{F}$ of size $2^{\ell'}$, where $\ell' = \delta \cdot \log_2 n$, and let $m = \log_{|H|} k = \frac{\log_2 k}{\log_2 |H|} = d/\ell' = O(1/\delta)$.[17]

[17] The fact that the value $\ell' = \delta \cdot \log_2 n$ is used both for $\log_2 |H|$ and for the distance between layers that we relate is a consequence of the fact that both parameters are

For each $i \in \{0,1,...,d-1\}$, viewing α_i as a function from $H^m \equiv [k]$ to $\{0,1\}$, the prover encodes α_i by a low degree polynomial $\widehat{\alpha}_i : \mathcal{F}^m \to \mathcal{F}$ that extends it (i.e., $\widehat{\alpha}_i(\sigma) = \alpha_i(\sigma)$ for every $\sigma \in H^m$); that is,

$$\widehat{\alpha}_i(z_1,...,z_m) = \sum_{\sigma_1,...,\sigma_m \in H} \mathtt{EQ}(z_1 \cdots z_m, \sigma_1 \cdots \sigma_m) \cdot \alpha_i(\sigma_1,...,\sigma_m) \tag{15}$$

where $\mathtt{EQ}$ is a low degree polynomial in the z_i's that tests equality over H^m (i.e., $\mathtt{EQ}(z_1 \cdots z_m, \sigma_1 \cdots \sigma_m) = \prod_{i \in [m]} \mathtt{EQ}_{\sigma_i}(z_i)$ and $\mathtt{EQ}_\sigma(z) = \prod_{\beta \in H \setminus \{\sigma\}} (z-\beta)/(\sigma - \beta)$). Actually, recalling that all but the first 2^i gates of layer i evaluate to 0, we re-write Eq. (15), for i's that are multiples of ℓ', as

$$\widehat{\alpha}_{i' \cdot \ell'}(z_1,...,z_m) = \sum_{\sigma_1,...,\sigma_{i'} \in H} \mathtt{EQ}(z_1 \cdots z_m, 1^{m-i'} \sigma_1 \cdots \sigma_{i'}) \cdot \alpha_i(1,...,1,\sigma_1,...,\sigma_{i'}) \tag{16}$$

Either way, $\widehat{\alpha}_i$ is a polynomial of individual degree $|H|-1$.

In light of the foregoing, proving that $C_n(x) = 1$ is equivalent to proving that $\widehat{\alpha}_0(1^m) = 1$, where $1^m \in H^m$ corresponds to the fixed (e.g., first) location of the output gate in the zero layer. This proof is conducted in $t = d/\ell'$ iterations, where in each iteration a multi-round interactive protocol is employed. Specifically, in i^{th} iteration, the correctness of the claim $\widehat{\alpha}_{(i-1)\cdot\ell'}(\overline{r}_{i-1}) = v_{i-1}$, where $\overline{r}_{i-1} \in \mathcal{F}^m$ and $v_{i-1} \in \mathcal{F}$ are known to both parties, is reduced (via the interactive protocol) to the claim $\widehat{\alpha}_{i\cdot\ell'}(\overline{r}_i) = v_i$, where $\overline{r}_i \in \mathcal{F}^m$ and $v_i \in \mathcal{F}$ are determined (by this protocol) such that both parties get these values. We stress that, with the exception of $i = t$, the $\widehat{\alpha}_{i\cdot\ell'}$'s are not known (or given) to the verifier; still, the claims made at the beginning (and at the end) of each iteration are well defined (i.e., each claim refers to a predetermined low degree polynomial that extends the values assigned to the gates (of a certain layer) of the circuit in a computation of the circuit on input $x \in \{0,1\}^n$).

Once the last iteration is completed, the verifier is left with a claim of the form $\widehat{\alpha}_d(\overline{r}_t) = v_t$, where $\widehat{\alpha}_d$ is defined as in Eq. (13). Recall that Eq. (13) has the form $\widehat{\alpha}_d(y) = \sum_{k \in \{0,1\}^\ell} \mathtt{EQ}(y,k) \cdot \mathtt{I}(k)$, where $\mathtt{I}(z) \stackrel{\text{def}}{=} \sum_{v \in [n+2]} \mathtt{EQ}(v, \widehat{\pi}(z)) \cdot x_v$ and $\widehat{\pi}$ is polynomial that is obtained by transforming the Boolean formula that computes π to a corresponding arithmetic formula. Hence, the verifier cannot evaluate $\widehat{\alpha}_d$ by itself, but it can verify its value via the Sum-Check protocol, since $\mathtt{I}$ is a low degree polynomial that can be evaluated in almost linear (in n) time. So, at this point, the parties run the Sum-Check protocol (see the last paragraph in Section 2.5).

A single iteration. The core of the iterative proof is the interactive protocol that is performed in each iteration. This protocol is based on the relation between

subject to the same trade-off. Each of these parameters cuts the number of rounds by its value (i.e., ℓ'), while incuring an exponential overhead (i.e., $2^{\ell'}$) in the total volume of communication.

subsequent α_i's, which is based on the canonical structure of the circuit. Specifically, recall that the i^{th} iteration reduces a claim regarding $\widehat{\alpha}_{(i-1)\cdot\ell'}$ to a claim regarding $\widehat{\alpha}_{i\cdot\ell'}$, where these polynomials encode the values of the corresponding layers in the circuit (i.e., layers $(i-1)\cdot\ell'$ and $i\cdot\ell'$). The relation between these layers is given by the following equation that relates the value at a specific (non-dummy) gate of level $(i-1)\cdot\ell'$ to the value of $2^{\ell'} = |H|$ gates of layer $i\cdot\ell'$:

$$\alpha_{(i-1)\cdot\ell'}(1^{m-(i-1)}, u_1, ..., u_{i-1}) = \mathtt{NAND}_{\ell'}((\alpha_{i\cdot\ell'}(1^{m-i}, u_1, ..., u_{i-1}, u))_{u\in H}) \quad (17)$$

where $1, u_1, ..., u_{i-1} \in H \equiv \{0,1\}^{\ell'}$ and $\mathtt{NAND}_{\ell'}$ is as defined in Eq. (14). Combining Eq. (16) with Eq. (17), it holds that $\widehat{\alpha}_{(i-1)\cdot\ell'}(z_1, ..., z_m)$ equals

$$\sum_{u_1,...,u_{i-1}\in H} \mathtt{EQ}(z_1\cdots z_m, 1^{m-i+1}u_1\cdots u_{i-1}) \cdot \mathtt{NAND}_{\ell'}((\widehat{\alpha}_{i\cdot\ell'}(1^{m-i}, u_1, ..., u_{i-1}, u))_{u\in H}). \quad (18)$$

In preparation to applying the Sum-Check protocol to Eq. (18), we observe that the corresponding $(i-1)$-variate polynomial is of individual degree $O(2^{\ell'}\cdot|H|) = O(n^{2\delta})$. This is the case because, for any fixed point $(\overline{r}', \overline{r}'') \in \mathcal{F}^{m-i+1} \times \mathcal{F}^{i-1}$, we can write Eq. (18) as

$$\begin{aligned}
&\mathtt{EQ}(\overline{r}', 1^{m-i+1}) \cdot \sum_{u_1,...,u_{i-1}\in H} \mathtt{EQ}(\overline{r}'', u_1\cdots u_{i-1}) \cdot \mathtt{NAND}_{\ell'}((\widehat{\alpha}_{i\cdot\ell'}(1^{m-i}, u_1, ..., u_{i-1}, u))_{u\in H}) \\
&= \mathtt{EQ}(\overline{r}', 1^{m-i+1}) \cdot \sum_{u_1,...,u_{i-1}\in H} P_{\overline{r}''}(u_1, ..., u_{i-1}),
\end{aligned}$$

where $P_{\overline{r}''}(y_1, ..., y_{i-1}) \stackrel{\text{def}}{=} \mathtt{EQ}(\overline{r}'', y_1\cdots y_{i-1})\cdot\mathtt{NAND}_{\ell'}((\widehat{\alpha}_{i\cdot\ell'}(1^{m-i}, y_1, ..., y_{i-1}, u))_{u\in H})$ is a low degree $(i-1)$-variate polynomial; specifically, its individual degree is dominated by the product of the total degree of $\mathtt{NAND}_{\ell'}$ and the individual degree of $\widehat{\alpha}_{i\cdot\ell'}$, which are $2^{\ell'}$ and $|H|-1$, respectively.

Applying the Sum-Check protocol to Eq. (18) allows to reduce a claim regarding the value of $\widehat{\alpha}_{(i-1)\cdot\ell'}$ at a specific point $\overline{r}_{i-1} = (\overline{r}'_{i-1}, \overline{r}''_{i-1}) \in \mathcal{F}^{m-i+1} \times \mathcal{F}^{i-1}$ to a claim regarding the value of the polynomial $P_{\overline{r}''_{i-1}}$ at a random point $(r''_1, ..., r''_{i-1})$ in $\mathcal{F}^{i-1}$, which in turn depends on the values of $\widehat{\alpha}_{i\cdot\ell'}$ at $2^{\ell'}$ points in $\mathcal{F}^m$ (i.e., the points $((1, ..., 1, r''_1, ..., r''_{i-1}, u))_{u\in H})$).

To reduce this claim to a claim regarding the value of $\widehat{\alpha}_{i\cdot\ell'}$ at a single point, we let the prover send these $2^{\ell'}$ values and perform "batch verification" for them. Specifically, the prover provides a low degree polynomial that describes the value of $\widehat{\alpha}_{i\cdot\ell'}$ on the axis-parallel line that goes through these points, and the claim to be proved in the next iteration is that the value of $\widehat{\alpha}_{i\cdot\ell'}$ at a random point

on this line equals the value provided by the polynomial sent by the prover.[18] Hence, the full protocol that is run in iteration i is as follows.

Construction 3.2 (reducing a claim about $\widehat{\alpha}_{(i-1)\cdot\ell'}$ to a claim about $\widehat{\alpha}_{i\cdot\ell'}$): *For known $\overline{r}_{i-1} \in \mathcal{F}^m$ and $v_{i-1} \in \mathcal{F}$, the* entry claim *is $\widehat{\alpha}_{(i-1)\cdot\ell'}(\overline{r}_{i-1}) = v_{i-1}$. The parties proceed as follows.*

1. *Applying the Sum-Check protocol to the entry claim, when expanded according to Eq. (18), determines $\overline{r}' \in \mathcal{F}^{i-1}$ and a value $v \in \mathcal{F}$ such that the residual claim for verification is*

$$\mathtt{EQ}(\overline{r}_{i-1}, 1^{m-(i-1)}\overline{r}') \cdot \mathtt{NAND}_{\ell'}((\widehat{\alpha}_{i\cdot\ell'}(1,...,1,\overline{r}',u))_{u\in H}) = v. \tag{19}$$

2. *The prover sends a univariate polynomial p' of degree smaller than $m \cdot |H|$ such that $p'(z) = \widehat{\alpha}_i(1,...,1,\overline{r}',z)$.*
3. *Upon receiving the polynomial p', the verifier checks whether v equals*

$$\mathtt{EQ}(\overline{r}_{i-1}, 1^{m-(i-1)}\overline{r}') \cdot \mathtt{NAND}_{\ell'}((p'(u))_{u\in H}), \tag{20}$$

   and continues only if equality holds (otherwise it rejects).
4. *The verifier selects a random $r \in \mathcal{F}$, and sends it to the prover. Both parties set $\overline{r}_i = (1,...,1,\overline{r}',r)$ and $v_i = p'(r)$.*

The exit claim *is $\widehat{\alpha}_{i\cdot\ell'}(\overline{r}_i) = v_i$.*

The complexities of Construction 3.2 are dominated by the application of the Sum-Check protocol, which refers to a polynomial of degree $O(2^{\ell'}\cdot|H|) = O(n^{2\delta})$. In particular, this implies that the verifier's strategy can be implemented in time $\widetilde{O}(n^{2\delta})$, provided that $|\mathcal{F}| = \mathrm{poly}(n)$. In this case, the prescribed prover strategy (as defined in Construction 3.2) can be implemented in time $\widetilde{O}(2^{d(n)}) = \mathrm{poly}(n)$,

Recall that after the last iteration of Construction 3.2, the resulting claim is checked by the Sum-Check protocol (applied to Eq. (13)), which leaves the verifier with the task of evaluating $\mathtt{I}$, where $\mathtt{I}(z) \stackrel{\mathrm{def}}{=} \sum_{v\in[n+2]} \mathtt{EQ}(v,\widehat{\pi}(z))\cdot x_v$. Using the hypothesis regarding π, it follows that the verifier runs in $n^{1+o(1)}$-time. The round complexity of the i^{th} iteration of Construction 3.2 is $i \le m$, and so the total round complexity is $m\cdot m + m = O(d(n)/\delta\log n)^2$.

One can readily verify that if the entry claim is correct, then the exit claim is correct, whereas if the entry claim is false, then with probability at least $1 - O(m\cdot 2^{\ell'}\cdot|H|/|\mathcal{F}|)$ the exit claim is false. Recall that the soundness error of the entire protocol is upper-bounded by the probability that there exists an iteration in which the entry claim is false but the exist claim is true. Hence, the total soundness error is $O(n^{2\delta}/|\mathcal{F}|) = o(1)$.

[18] We mention that the fact that these $2^{\ell'}$ points reside on a line makes the argument simpler, but not in a fundamental way. In general, the prover could have picked a curve of degree $2^{\ell'}-1$ that goes through any $2^{\ell'}$ points of interest, and provide a low degree polynomial describing the value of $\widehat{\alpha}_{i\cdot\ell'}$ on this curve. In this case, the claim to be proved in the next iteration would have been that the value of $\widehat{\alpha}_{i\cdot\ell'}$ at a random point on this curve equals the value provided by the polynomial sent by the prover.

Appendix: The Sum-Check protocol

The Sum-Check protocol, designed by Lund, Fortnow, Karloff, and Nisan [12], is a key ingredient in the constructions that we present.

Fixing a finite field $\mathcal{F}$ and a set $H \subset \mathcal{F}$ (e.g., H may be a two-element set), we consider an m-variate polynomial $P : \mathcal{F}^m \to \mathcal{F}$ of individual degree d. Given a value v, the Sum-Check protocol is used to prove that

$$\sum_{\sigma_1,...,\sigma_m \in H} P(\sigma_1, ..., \sigma_m) = v, \tag{21}$$

assuming that the verifier can evaluate P by itself. The Sum-Check protocol proceeds in m iterations, such that in the i^{th} iteration the number of summations (over H) decreases from $m - i + 1$ to $m - i$. Specifically, the i^{th} iteration starts with a claim of the form $\sum_{\sigma_i,...,\sigma_m \in H} P(r_1, ..., r_{i-1}, \sigma_i, ..., \sigma_m) = v_{i-1}$, where $r_1, ..., r_{i-1}$ and v_{i-1} are as determined in prior iterations (with $v_0 = v$), and ends with a claim of the form $\sum_{\sigma_{i+1},...,\sigma_m \in H} P(r_1, ..., r_i, \sigma_{i+1}, ..., \sigma_m) = v_i$, where r_i and v_i are determined in the i^{th} iteration. Initializing the process with $v_0 = v$, in the i^{th} iteration the parties act as follows.

Prover's move: The prover computes a univariate polynomial of degree d over $\mathcal{F}$

$$P_i(z) \stackrel{\text{def}}{=} \sum_{\sigma_{i+1},...,\sigma_m \in H} P(r_1, ..., r_{i-1}, z, \sigma_{i+1}, ..., \sigma_m) \tag{22}$$

where $r_1, ..., r_{i-1}$ are as determined in prior iterations, and sends P_i to the verifier (claiming that $\sum_{\sigma \in H} P_i(\sigma) = v_{i-1}$).

Verifier's move: Upon receiving a degree d polynomial, denoted $\widetilde{P}$, the verifier checks that $\sum_{\sigma \in H} \widetilde{P}(\sigma) = v_{i-1}$ and rejects if inequality holds. Otherwise, it selects r_i uniformly in $\mathcal{F}$, and sends it to the prover, while setting $v_i \leftarrow \widetilde{P}(r_i)$.

If all m iterations are completed successfully (i.e., without the verifier rejecting in any of them), then the verifier conducts a final check. It computes the value of $P(r_1, ..., r_m)$ and accepts if and only if this value equals v_m.

Clearly, if Eq. (21) holds (and the prover acts according to the protocol), then the verifier accepts with probability 1. Otherwise (i.e., Eq. (21) does not hold), no matter what the prover does, the verifier accepts with probability at most $m \cdot d/|\mathcal{F}|$, because in each iteration if the prover provides the correct polynomial, then the verifier rejects (since $\sum_{\sigma \in H} P_i(\sigma) = P_{i-1}(r_{i-1}) \neq v_{i-1}$), and otherwise the (degree d) polynomial sent agrees with P_i on at most d points.[19]

[19] If P_i does not satisfy the current claim (i.e., $\sum_{\sigma \in H} P_i(\sigma) \neq v_{i-1}$), then the prover can avoid upfront rejection only if it sends a degree d polynomial $\widetilde{P} \neq P_i$. But in such a case, $\widetilde{P}$ and P_i may agree on at most d points, since they are both degree d polynomials. Hence, if the chosen $r_i \in \mathcal{F}$ is not one of these points, it holds that $v_i = \widetilde{P}(r_i) \neq P_i(r_i)$, which means that the next iteration will also start with a false claim. Hence, starting with a false claim (i.e., $\sum_{\sigma \in H} P_1(\sigma) \neq v_0$ since Eq. (21) does not hold), with probability at least $1 - m \cdot d/|\mathcal{F}|$, after m iterations we reach a false claim regarding the value of P at a single point.

The complexity of verification is dominated by the complexity of evaluating P (on a single point). As for the prescribed prover, it may compute the relevant P_i's by interpolation, which is based on computing the value of P at $(d+1) \cdot |H|^{m-i}$ points, for each $i \in [m]$. (That is, the polynomial P_i is computed by obtaining its values at $d+1$ points, where the value of P_i at each point is obtained by summing the values of P at $|H|^{m-i}$ points.)[20]

Acknowledgements

As noted in the body of the paper, an unpublished work by Yael Kalai and Guy Rothblum [11] proposed a constant-round doubly-efficient proof system for $\mathcal{NC}^1$ under a very strict notion of uniformity. This unpublished work has inspired our own work, and we thank Yael for her contribution to it as well as for many other helpful conversations on these topics.

References

1. Noga Alon, Oded Goldreich, Johan Hastad, and Rene Peralta. Simple Construction of Almost k-wise Independent Random Variables. *Random Structures and Algorithms*, Vol. 3 (3), pages 289–304, 1992.
2. David A. Mix Barrington, Neil Immerman, and Howard Straubing. On Uniformity within NC1. *Journal of Computer and System Science*, Vol. 41 (3), pages274–306, 1990.
3. Oded Goldreich. *Computational Complexity: A Conceptual Perspective*. Cambridge University Press, 2008.
4. Oded Goldreich. On the doubly-efficient interactive proof systems of GKR. *ECCC*, TR17-101, 2017.
5. Oded Goldreich and Guy N. Rothblum. Simple doubly-efficient interactive proof systems for locally-characterizable sets. *ECCC*, TR17-018, 2017.
6. Oded Goldreich and Guy N. Rothblum. Worst-case to Average-case reductions for subclasses of P. *ECCC* TR17-130, 2017.
7. Oded Goldreich and Guy N. Rothblum. Counting t-cliques: Worst-case to average-case reductions and direct interactive proof systems. *ECCC* TR18-046, 2018.
8. Shafi Goldwasser, Yael Tauman Kalai, and Guy N. Rothblum. Delegating Computation: Interactive Proofs for Muggles. *Journal of the ACM*, Vol. 62(4), Art. 27:1-27:64, 2015. Extended abstract in *40th STOC*, pages 113–122, 2008.
9. Shafi Goldwasser, Silvio Micali, and Charles Rackoff. The Knowledge Complexity of Interactive Proof Systems. *SIAM Journal on Computing*, Vol. 18, pages 186–208, 1989. Preliminary version in *17th STOC*, 1985.
10. Yael Tauman Kalai and Ran Raz. Interactive PCP. In *35th International Colloquium on Automata, Languages and Programming* (Part II), pages 536–547, 2008.
11. Yael Tauman Kalai and Guy N. Rothblum. Constant-round interactive proofs for NC1. Unpublished observation, 2009.

[20] Specifically, the value of P_i at p is obtained from the values of P at the points $(r_1, ..., r_{i-1}, p, \sigma)$, where $\sigma \in H^{m-i}$.

12. Carsten Lund, Lance Fortnow, Howard Karloff, and Noam Nisan. Algebraic methods for interactive proof systems. *Journal of the ACM*, Vol. 39, No. 4, pages 859–868, 1992. Extended abstract in *31st FOCS*, 1990.
13. Joseph Naor and Moni Naor. Small-Bias Probability Spaces: Efficient Constructions and Applications. *SIAM Journal on Computing*, Vol. 22 (4), pages 838–856, 1993. Preliminary version in *22nd STOC*, 1990.
14. Alexander A. Razborov. Lower bounds on the size of bounded-depth networks over a complete basis with logical addition. In *Matematicheskie Zametki*, Vol. 41, No. 4, pages 598–607, 1987 (in Russian). English translation in *Mathematical Notes of the Academy of Sci. of the USSR*, Vol. 41 (4), pages 333–338, 1987.
15. Omer Reingold, Guy N. Rothblum, and Ron D. Rothblum. Constant-round interactive proofs for delegating computation. In *48th ACM Symposium on the Theory of Computing*, pages 49–62, 2016.
16. Adi Shamir. IP = PSPACE. *Journal of the ACM*, Vol. 39, No. 4, pages 869–877, 1992. Preliminary version in *31st FOCS*, 1990.
17. Roman Smolensky. Algebraic Methods in the Theory of Lower Bounds for Boolean Circuit Complexity. In *19th ACM Symposium on the Theory of Computing* pages 77–82, 1987.
18. Ryan Williams. Faster all-pairs shortest paths via circuit complexity. In *46th ACM Symposium on the Theory of Computing*, pages 664–673, 2014.